

General Description

The AO4618 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This complementary N and P channel MOSFET configuration is ideal for low Input Voltage inverter applications.

Product Summary

N-Channel

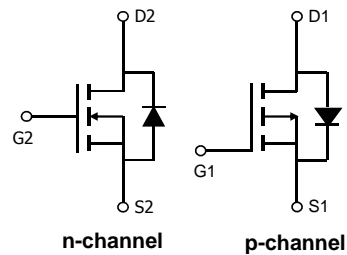
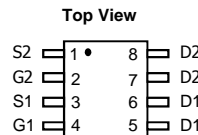
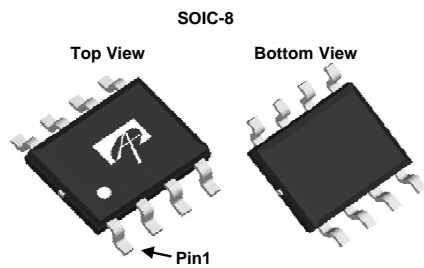
$V_{DS} = 40V$
 $I_D = 8A$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 19m\Omega$ ($V_{GS} = 10V$)
 $< 27m\Omega$ ($V_{GS} = 4.5V$)

100% UIS Tested
 100% R_g Tested

P-Channel

$-40V$
 $-7A$ ($V_{GS} = -10V$)
 $R_{DS(ON)} < 23m\Omega$ ($V_{GS} = -10V$)
 $< 30m\Omega$ ($V_{GS} = -4.5V$)

100% UIS Tested
 100% R_g Tested



Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current	I_D	$T_A = 25^\circ C$	8	A
		$T_A = 70^\circ C$	6	
Pulsed Drain Current ^C	I_{DM}	40	-35	A
Avalanche Current ^C	I_{AS}	15	-35	A
Avalanche energy $L = 0.1mH$ ^C	E_{AS}	11	61	mJ
Power Dissipation ^B	P_D	$T_A = 25^\circ C$	2	W
		$T_A = 70^\circ C$	1.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	48	62.5	$^\circ C/W$
Maximum Junction-to-Ambient ^{A,D}		Steady-State	74	90
Maximum Junction-to-Lead	$R_{\theta JL}$	32	40	$^\circ C/W$

N-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.4	1.9	2.4	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =8A T _J =125°C		15.4	19	mΩ
		V _{GS} =4.5V, I _D =4A		21	27	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =8A		33		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.75	1	V
I _S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, f=1MHz		415		pF
C _{oss}	Output Capacitance			112		pF
C _{riss}	Reverse Transfer Capacitance			11		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1	2.2	3.5	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =8A		6.5	12	nC
Q _{g(4.5V)}	Total Gate Charge			3	6	nC
Q _{gs}	Gate Source Charge			1.2		nC
Q _{gd}	Gate Drain Charge			1.1		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =20V, R _L =2.5Ω, R _{GEN} =3Ω		4		ns
t _r	Turn-On Rise Time			3		ns
t _{D(off)}	Turn-Off DelayTime			15		ns
t _f	Turn-Off Fall Time			2		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =8A, dI/dt=100A/μs		12.5		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =8A, dI/dt=100A/μs		3.5		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

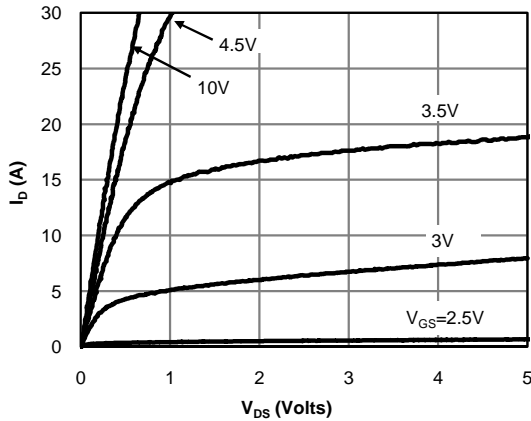


Fig 1: On-Region Characteristics (Note E)

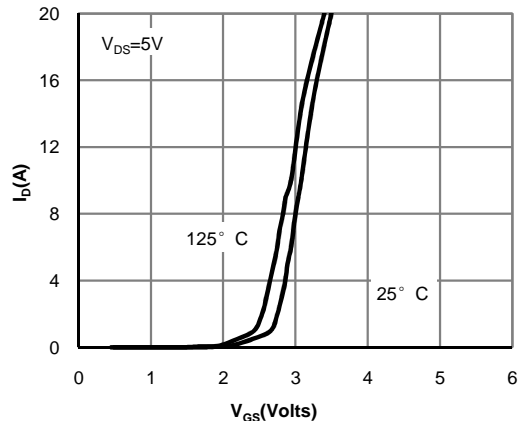


Figure 2: Transfer Characteristics (Note E)

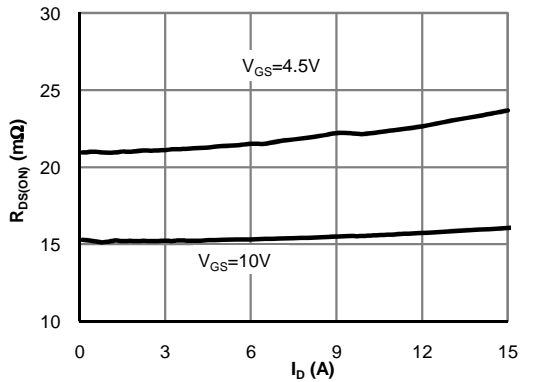


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

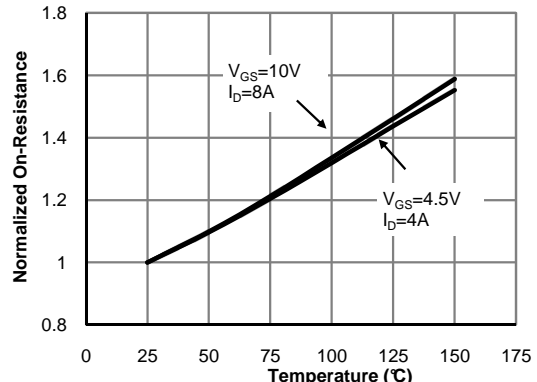


Figure 4: On-Resistance vs. Junction Temperature (Note E)

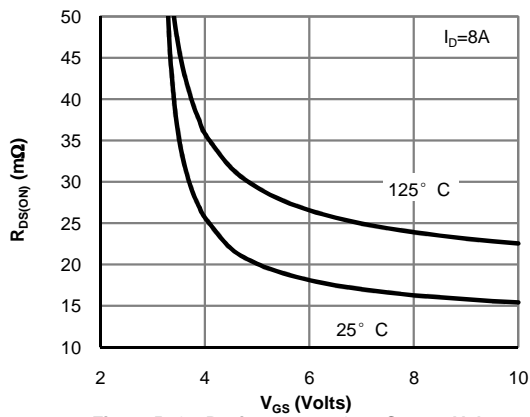


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

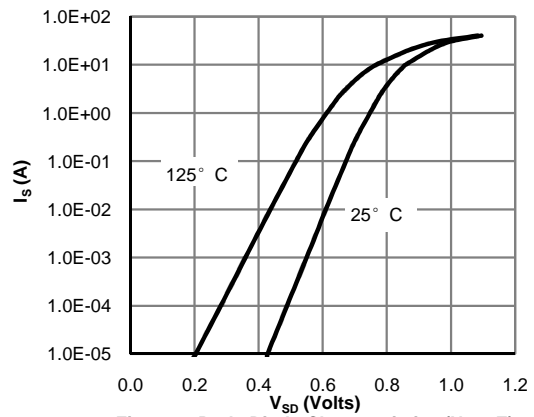


Figure 6: Body-Diode Characteristics (Note E)

N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

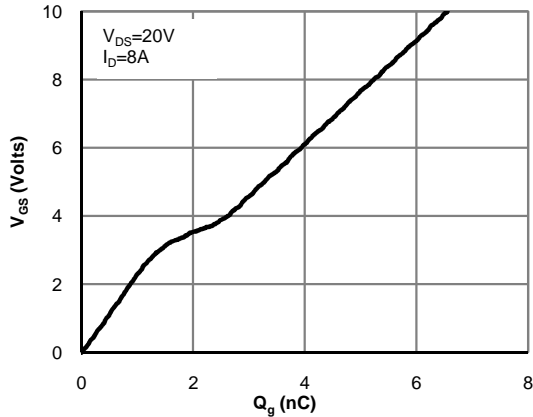


Figure 7: Gate-Charge Characteristics

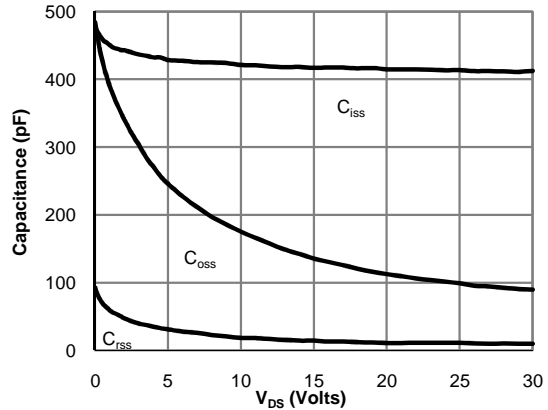


Figure 8: Capacitance Characteristics

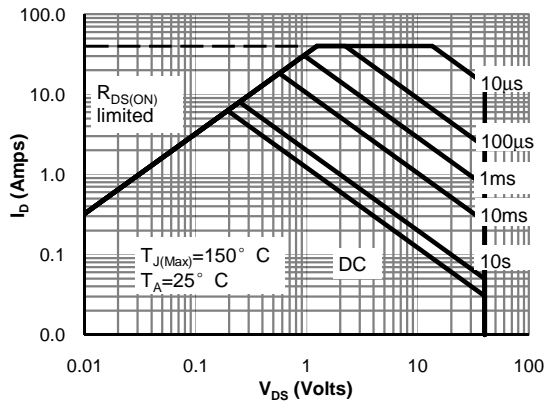


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

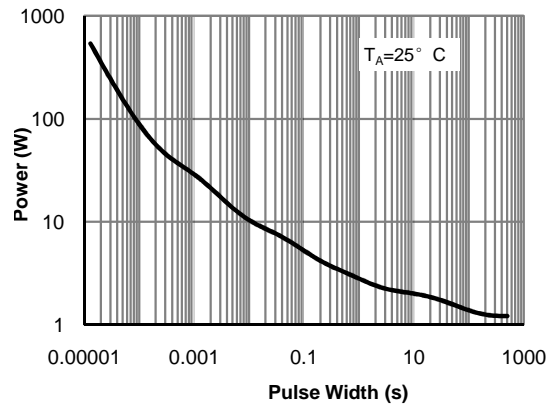


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

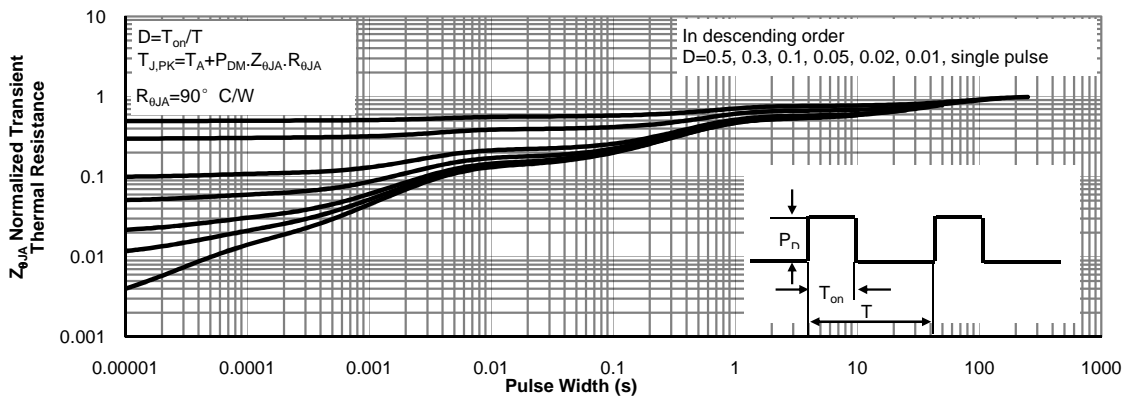
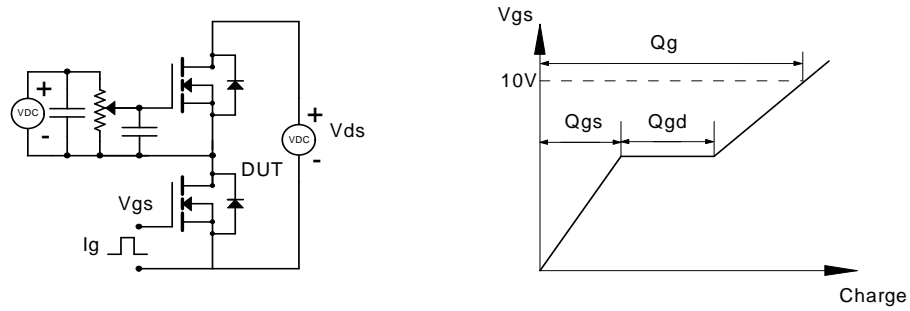
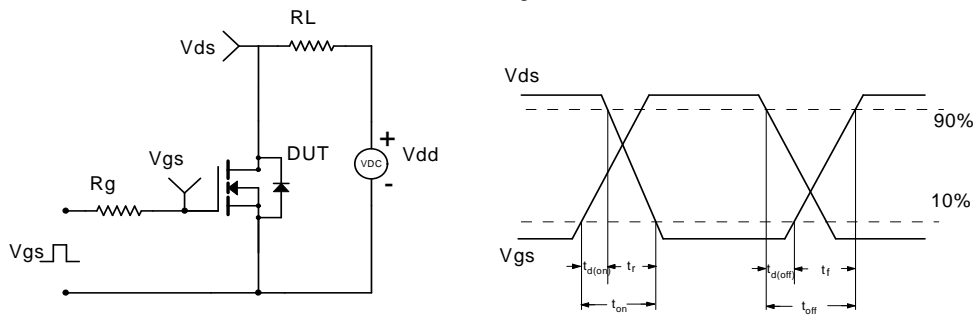


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

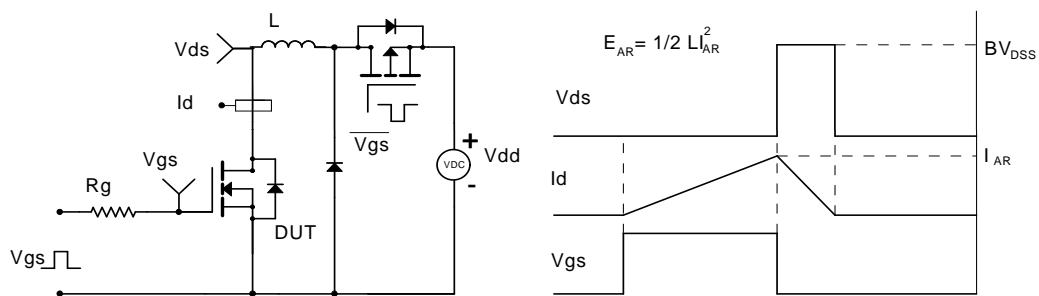
Gate Charge Test Circuit & Waveform



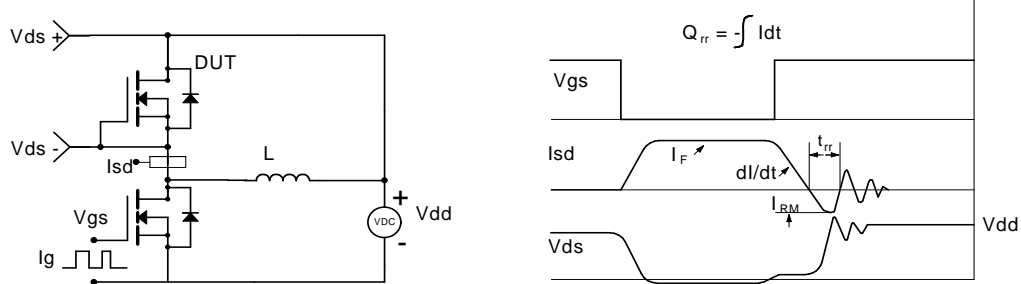
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-40V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.7	-1.9	-3	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-7A T _J =125°C		19	23	mΩ
		V _{GS} =-4.5V, I _D =-4A		28.5	35	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-7A		26		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.74	-1	V
I _S	Maximum Body-Diode Continuous Current				-2.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-20V, f=1MHz		1870		pF
C _{oss}	Output Capacitance			185		pF
C _{riss}	Reverse Transfer Capacitance			155		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		4.5	9	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =-20V, I _D =-7A		32	45	nC
Q _g (4.5V)	Total Gate Charge			8	12	nC
Q _{gs}	Gate Source Charge			7.6		nC
Q _{gd}	Gate Drain Charge			6.2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =-20V, R _L =2.8Ω, R _{GEN} =3Ω		10		ns
t _r	Turn-On Rise Time			18		ns
t _{D(off)}	Turn-Off DelayTime			38		ns
t _f	Turn-Off Fall Time			24		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-7A, dI/dt=500A/μs		13		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-7A, dI/dt=500A/μs		33		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

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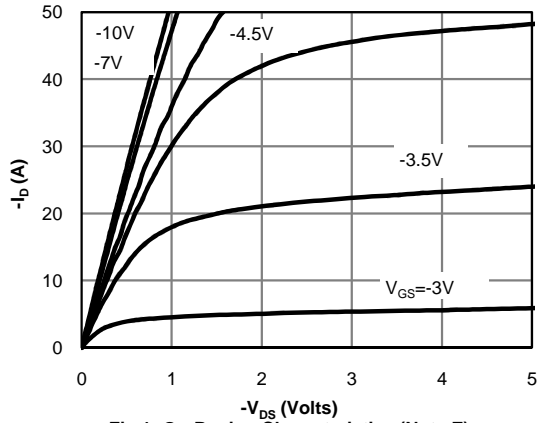


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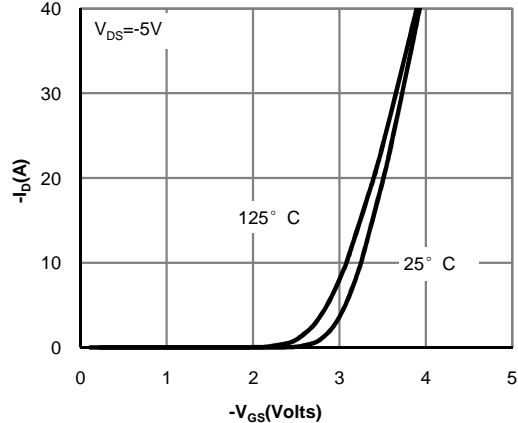


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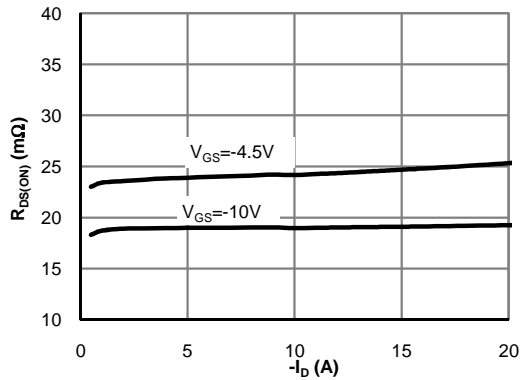


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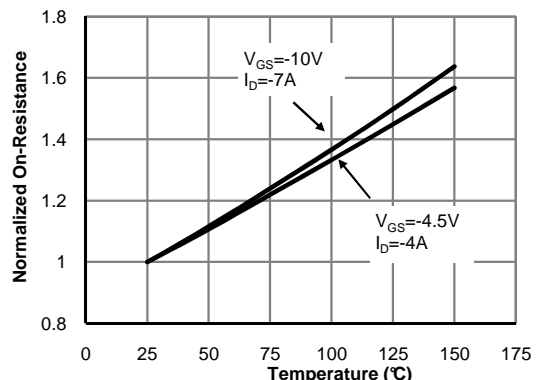


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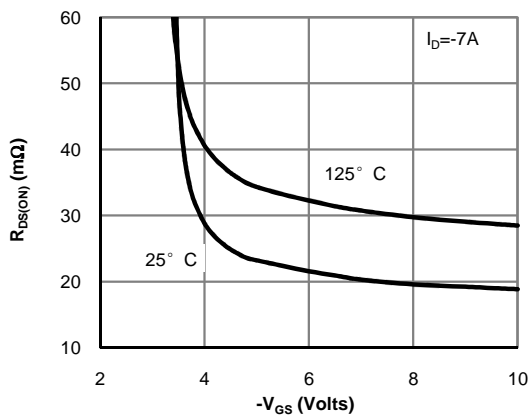


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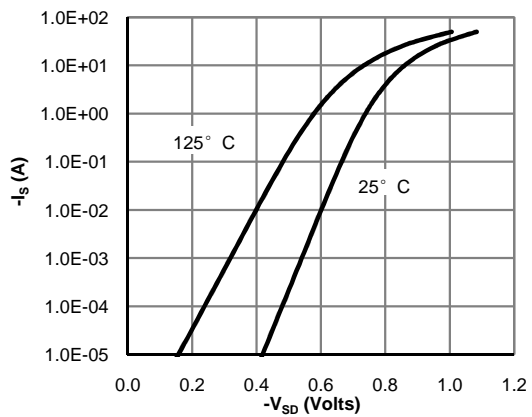


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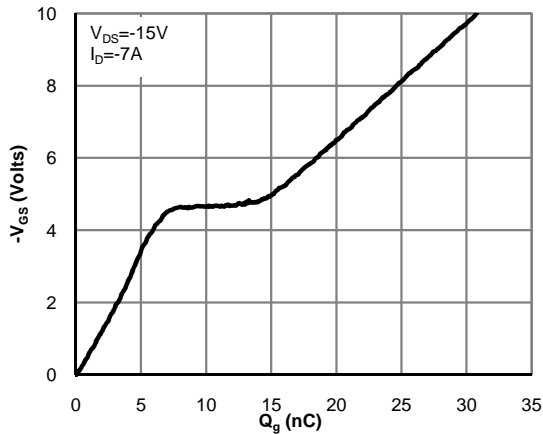


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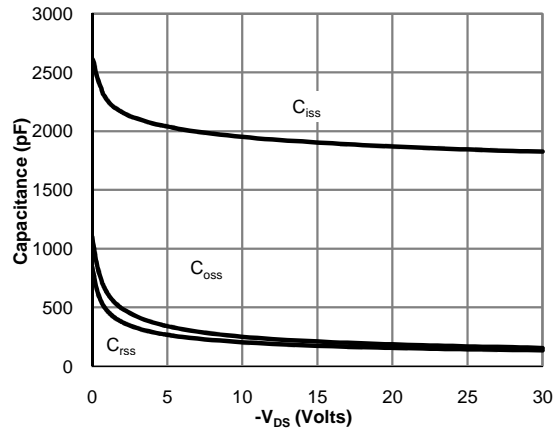


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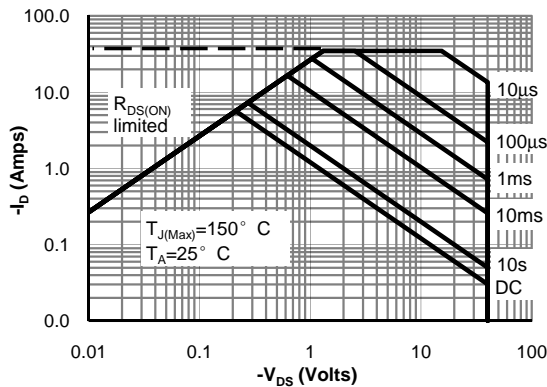


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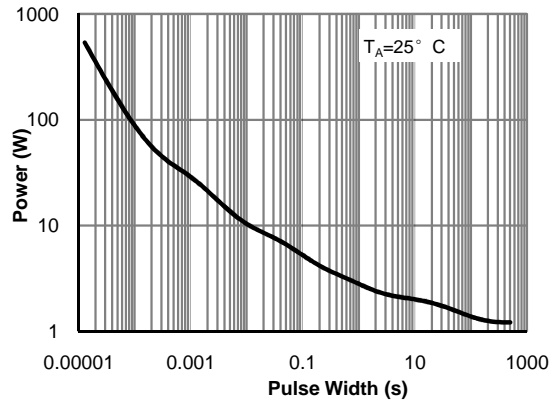


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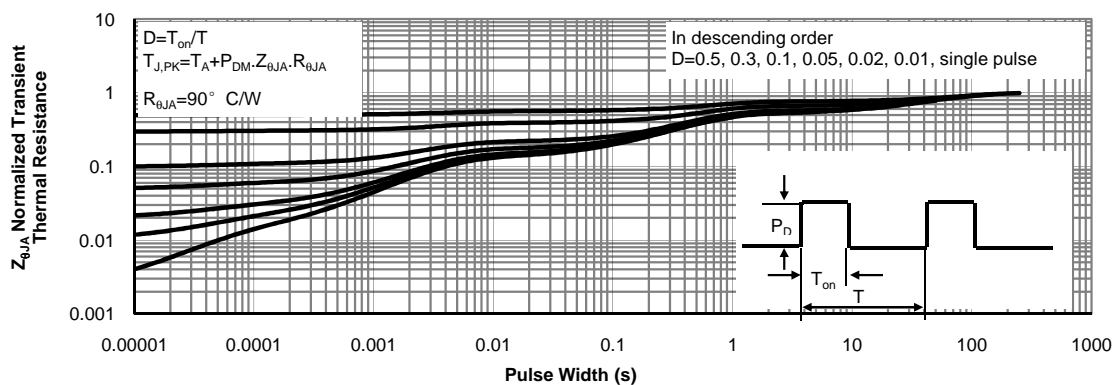
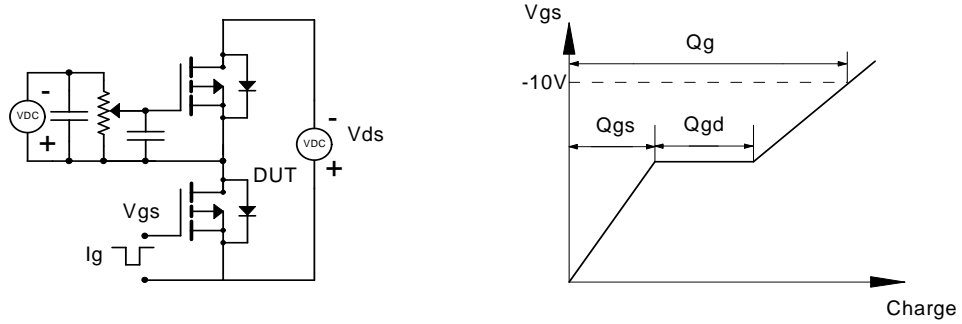
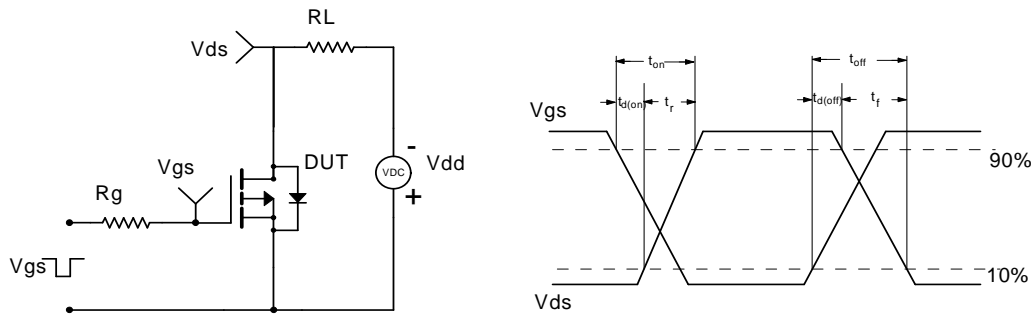


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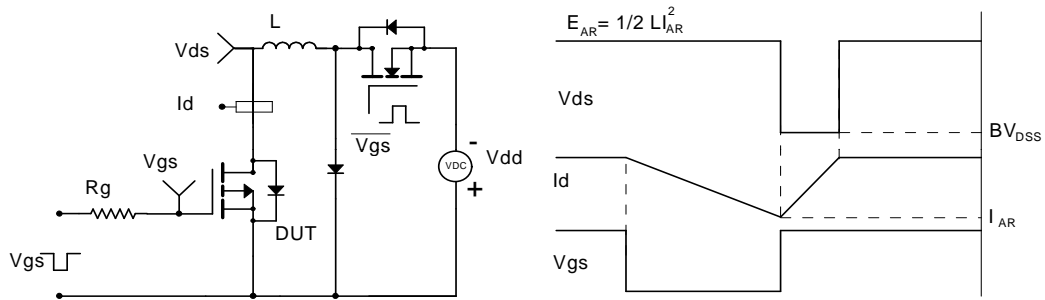
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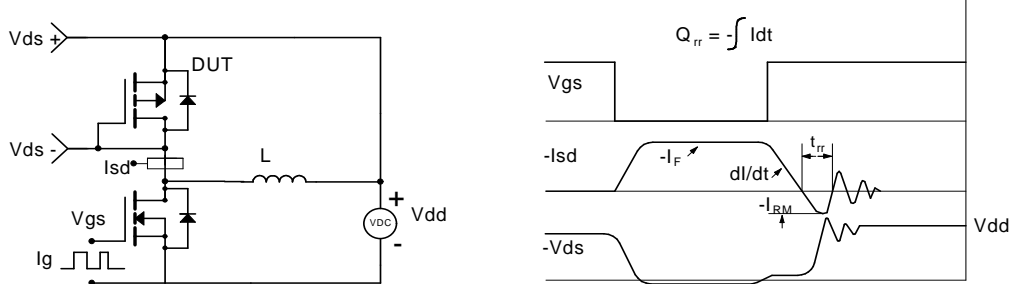
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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